**Digital System Design**

**ASSIGNMENT REPORT**

**TEAM MEMBERS:**

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**TEAM NUMBER : 66**

**1- THE IDEA:**

-Design a 3-bit adder on the DE10-lite FPGA board using 6 switches (3 for each input). The sum should be displayed using 4 LEDS representing the 4-bit sum. Output the result on two of the 7-segment displays. (BCD addition)

**2-Components:**

1- ALTERA FPGA board

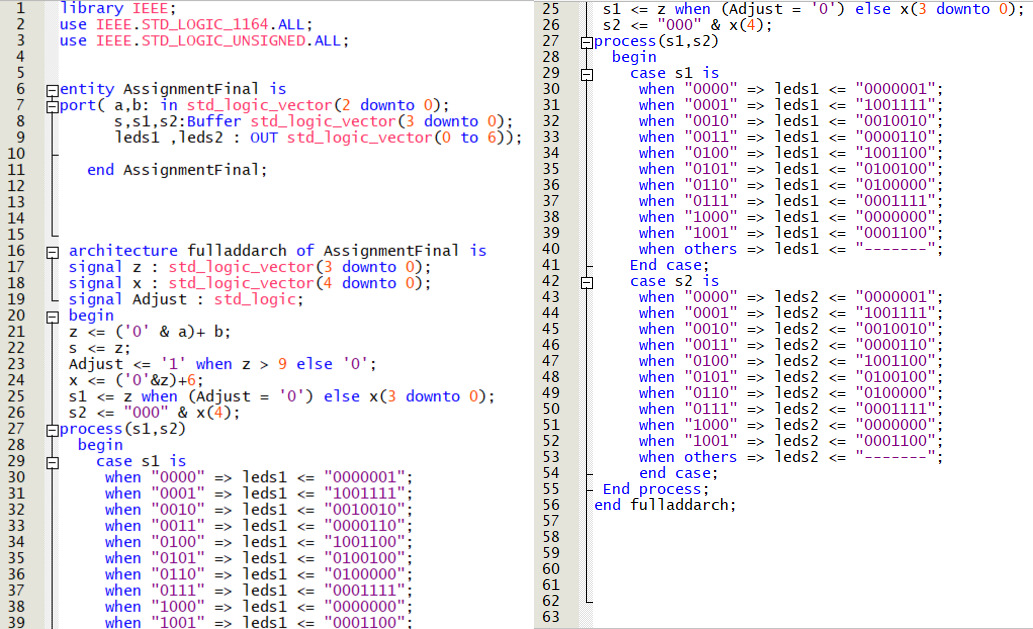
2- LEDs

3- Switches

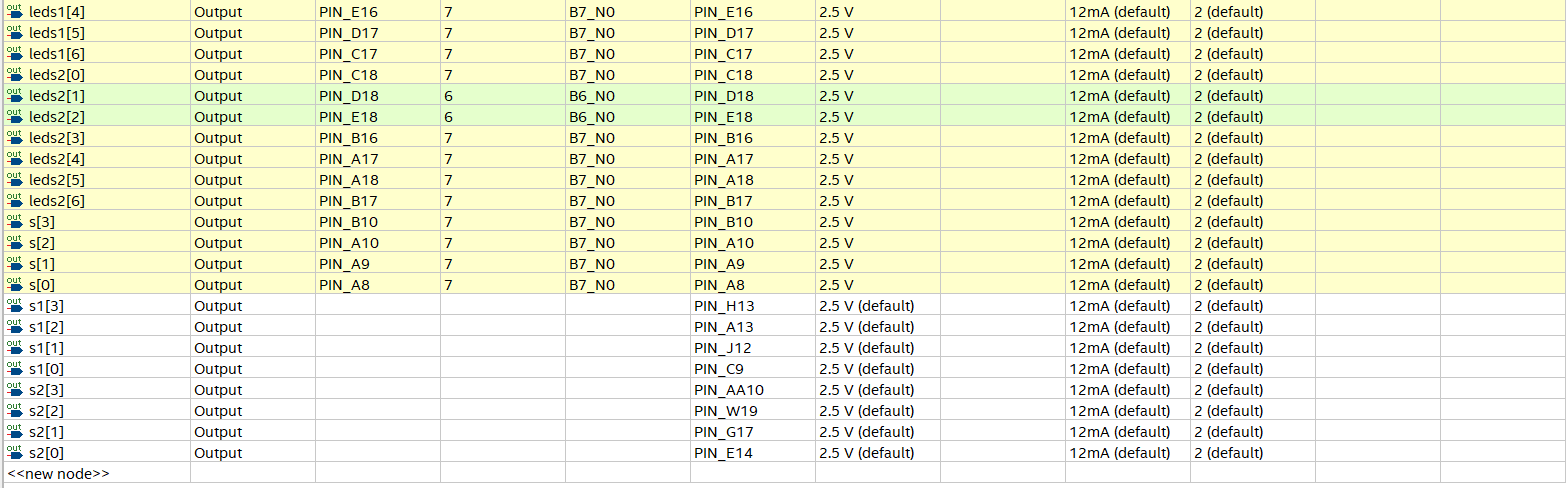
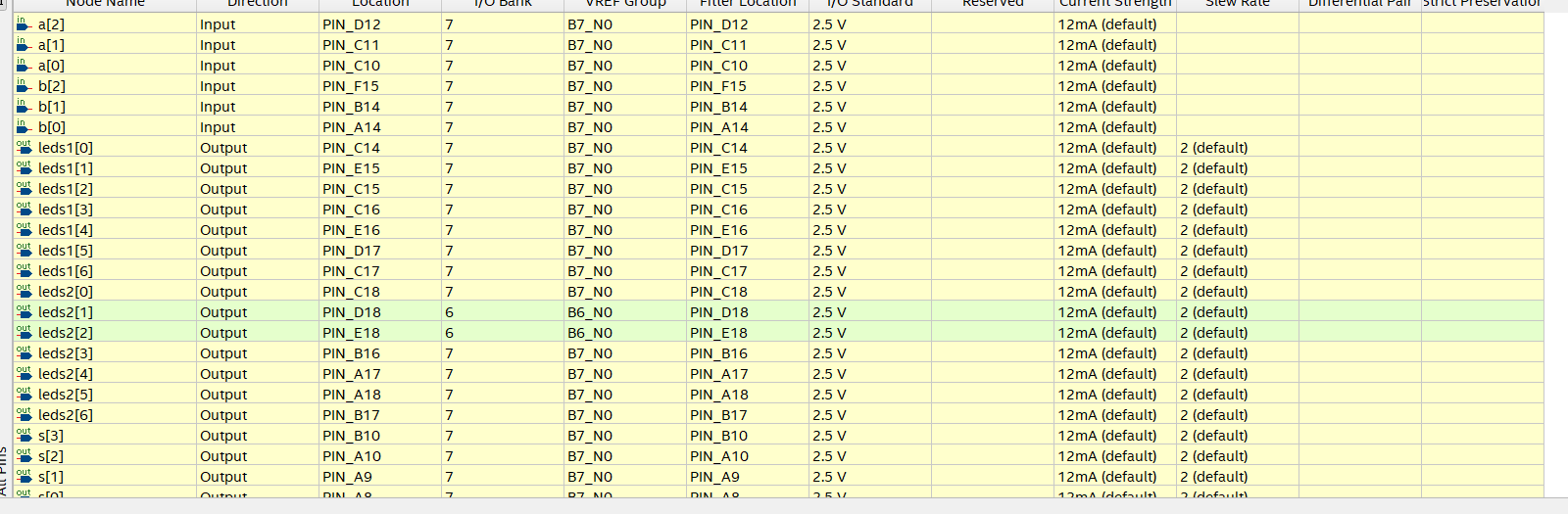
4- Seven segments

**3-THE IMPLEMENTATION:**

**1- CODE:**

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**1- PIN ASSIGNMENTS:**



**1- PIN TOPS:**

